

over *Berthoumieux* and *Scott* as applied to the above rejection, and in further view of *Krasner* (U.S. Patent No. 5,841,396); claims 11-26 stand rejected under §103(a) as being unpatentable over *Berthoumieux* in view of *Scott* and *Krasner*; and claims 27-28 stand rejected under §103(a) as being unpatentable over *Berthoumieux* in view of *Krasner*.

Applicant respectfully traverses each of these rejections. Each of these rejections is based on a flawed rationale involving the combination of *Berthoumieux* in view of *Scott* and/or *Krasner*; Applicant submits that the rationale is flawed generally because: (1) the Office Action has misrepresented the asserted prior art; (2) the Office Action's proposed modifications to *Berthoumieux* (in view of *Scott* and/or *Krasner*) would undermine the purpose and operation of *Berthoumieux*; and (3) in attempting to hindsight reconstruct the claimed invention via the teachings of *Berthoumieux* and *Scott*, the Office Action failed to cite evidence in support of the notion that the skilled artisan would be led by the prior art to modify the teachings of *Berthoumieux* as asserted in the Office Action.

(1) The Office Action Has Misrepresented The Prior Art Including *Scott*

With respect to the first three rejections, Applicant respectfully submits that the Office Action has misrepresented the prior art as well as *Scott*. The Office Action uses a misinterpretation of *Scott* in an attempt to support the erroneous argument that "it is well known that the digital processing circuitry of a radio communications device can process data much faster than the analog circuitry can capture the incoming data." This statement is untrue as evidenced by the fact that digital signal processing is merely the manipulation of samples of analog signals. Moreover, as evidenced by any technical dictionary, it is a signal-processing axiom that "digital signals" in such environments are merely sampled snap shots of the analog signal. Moreover, a digital signal processor usually consumes several clock periods in order to process a single sample of an already-captured analog signal.

The Office Action attempts to support this erroneous "well-known" prior-art characterization by presenting two illogical and erroneous statements in relation to *Scott*. First, the Office Action alleges that *Scott*'s Figure 1 shows a delay period 106 and that this delay period is also the guard interval. Contrary to this representation in the Office Action, *Scott* explains that the guard time and the delay period are two different entities; the "TDD guard time is a fixed

length, determined by cell radius, while the actual round trip frame duration varies according to the distance to the user station.” See *Scott* at column 3, lines 6-7. At column 2, lines 30-35 and 61-64, *Scott* explains and Figure 2 illustrates that the delay period 106 is primarily the base-transmission propagation time. Second, contrary to the Office Action, neither at column 2, lines 25-35, nor anywhere else in relation to Figures 1 or 2, does *Scott* teach anything that would relate to or support the statement: “Hence, the time it takes for the data to be processed by a DSP, which occurs during this guard time, is less than the time necessary for the analog portion of the circuitry to capture the information.” In relation to Figures 1 and 2, *Scott* does not teach anything substantive about the time it takes for data to be processed by a DSP relative to propagation and delay times.

Hence, the rationale provided at page 3 of the Office Action, and which supports each such rejection, is in error; therefore, each rejection is flawed and should be removed.

(2) The Proposed Modification To *Berthoumieux* Would Undermine *Berthoumieux*

The purpose of the embodiment taught by *Berthoumieux* is to reduce clock-harmonic disturbances of received low-level radio signals in receiver applications where a digital processing unit uses a high-speed clock having second- or third-order harmonics in the vicinity of the carrier frequency of the received low-level radio signals. See *Berthoumieux* at page 2, lines 3, *et seq.* *Berthoumieux* attempts to avoid these clock-harmonic disturbances “by lowering the speed of functioning of at least one clock associated with this digital processing unit” during time when the ADC 5 is processing data. See *Berthoumieux* at page 3. The particular embodiment relied upon for the rejections is shown as *Berthoumieux*’s sole Figure; in this illustrated embodiment, the time control component 4 is shown containing a master clock which, in turn, is the uninterrupted source for the ADC 5 and also the controlled source for the DSP clock(s). See *Berthoumieux* at page 3, lines 19, *et seq.*

For the first three rejections, according to the Office Action, the skilled artisan would read the *Berthoumieux* reference and would be led by the prior art to set “the time [master-clock] control component 4 such that the period, during which the data is processed by the DSP, occurs during a shorter time interval than the period during which the incoming data stream is captured by the analog circuitry and the DSP is in a reduced activity mode in order to increase system

efficiency....” As pointed out above, this teaching is not found in the prior art. Furthermore, this proposed modification to *Berthoumieux* would change the embodiment taught by *Berthoumieux* so that, instead of permitting the master-clock control component 4 to drive the ADC 5 uninterrupted, the master-clock control component 4 would drive the ADC 5 for certain periods that are longer than periods during which the master-clock control component 4 would drive the DSP clock(s). Because this master-clock control component 4 only responds to the detection means 8, it would have no sensing circuitry for differentiating these different times when it would purportedly drive the ADC 5 and the DSP clock(s). Consequently, the Office Action’s modification proposed for the *Berthoumieux* embodiment would have *Berthoumieux*’s master-clock control component 4 responding to the detection means 8 by interrupting the clock source for the ADC 5 (and thereby lose the data therethrough) when the purported new objective would be to interrupt the clock source for the DSP clock(s). Accordingly, the Office Action’s modification proposed would undermine the purpose and operation of the *Berthoumieux* embodiment. According to long-standing case law, a §103 rejection cannot be maintained when the proposed modification undermines purpose of main reference; the prior art would teach away from such a proposed modification. See, e.g., *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

With respect to the fourth rejection in which the combined teachings of *Berthoumieux* and *Krasner* are relied upon, as with the discussion above, the Office Action fails to appreciate that the time control component 4 of *Berthoumieux* only responds and reacts to instants when data is being received and processed by the ADC 5; therefore, the proposed modification based on *Krasner* would not permit for disabling of the ADC 5 without entirely undermining the objective and operation of *Berthoumieux*. As discussed above, *Berthoumieux*’s purpose is to reduce clock-harmonic disturbances of received low-level radio signals in receiver applications where a digital processing unit uses a high-speed clock having second- or third-order harmonics in the vicinity of the carrier frequency of the received low-level radio signals. By disabling the ADC 5, the time control component 4 of *Berthoumieux* would not be able to respond and react to instants when data is being received and processed by the ADC 5; in effect, the Office Action’s proposed modification would result in a locked-up circuit. Thus, the §103 rejection cannot be maintained

because the proposed modification would undermine both the purpose and operation of *Berthoumieux*.

(3) Each Of The Prior-Art Rejections Fails To Cite Evidence For The Proposed Modifications

Applicant respectfully submits that each of the rejections is based on improper hindsight reconstruction directed at the claimed invention. None of the rejections cites any discussion in the prior art that would suggest the proposed combination. However, such evidence in the prior art is required in order to maintain a §103 rejection. As set forth in *Ruiz v. A.B. Chance Co.*, 234 F.3d 654 (December 6, 2000), the alleged motivation for combining the references is to be suggested by the *references* themselves: "Our court has provided [that the] motivation to combine may be found explicitly or implicitly: 1) in the *prior art references* themselves; 2) in the knowledge of those of ordinary skill in the art that certain *references*, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to *references* relating to possible solutions to that problem.'"

In relation to each of the four prior-art rejections, no evidence in the prior art was cited as support for the proposed combination.

In view of the above, Applicant submits that each of the claims is in condition for allowance. Reconsideration and withdrawal of the rejections, along with a favorable response, are earnestly requested.

Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at 651/686-6633.

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